P. 02

MAR-01-2005 TUE 08:46 AM AMD

FAX NO. 4087493718



Patent Attorney Docket No. H1105D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of) MAIL STOP AF
Shibly S. Ahmed et al.) Group Art Unit: 2812
Application No.: 10/602,061) Examiner: R. Pompey
Filed: June 24, 2003)
For: DOUBLE GATE SEMICONDUCTOR HAVING SEPARATE GATES))

DECLARATION UNDER 37 C.F.R. § 1.131

U.S. Patent and Trademark Office Customer Window, Mail Stop AF Randolph Building 401 Dulany Street Alexandria, Virginia 22314

Sir:

- I, Shibly S. Ahmed, an inventor of the subject matter claimed in the above-referenced application, hereby declare that:
- 1. An invention disclosure describing the invention was completed by me on August 16, 2002. The invention disclosure included five pages that describe the invention (See Exhibit A).
- 2. A letter dated August 29, 2002 was sent from Advanced Micro Devices, Inc. to the law firm of Harrity & Snyder, LLP indicating that the invention described in the invention disclosure had been approved for the preparation of a patent application (See Exhibit B).
- 3. A first draft of a patent application based on my invention disclosure was sent from Harrity & Snyder, ILP to me on October 1, 2002 via e-mail (See Exhibit C).

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U.S. Patent Application No. 10/602,061 Attorney Docket No. H1105D

- 4. I provided comments regarding the draft patent application to Harrity & Snyder, LLP via email on October 15, 2002. The completed U.S. Patent Application, along with Declaration/Power of Attorney and Assignment documents were sent to Advanced Micro Devices, Inc. for execution on October 17, 2002 via Federal Express (See Exhibit D).
- 5. The executed Declaration/Power of Attorney and Assignment documents were sent to Harrity & Snyder LLP via Federal Express on November 7, 2002 for filing along with the application (See Exhibit E).
- 6. The Utility Patent Application was filed in the United States Patent and Trademark Office on November 8, 2002.
- 7. My co-inventors on this application (Haihong Wang and Bin Yu) are no longer employed at Advanced Micro Devices, Inc.
- 8. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements made jeopardize the validity of the application or any patent issuing therefrom.

Date:	3.1.05	Signature: Shiply See	lique Ahmed
			7

Shibly S. Ahmed

MAR-01-2005 TUE 08:46 AM AMD FAX NO. 4087493718

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U.S. Patent Application No. 10/602,061 Attorney Docket No. H1105D

LIST OF EXHIBITS

- A. Copy of relevant portions of AMD Invention Disclosure prepared August 16, 2002.
- B. Copy of relevant portions of letter from AMD to Harrity & Snyder, LLP dated August 29, 2002 authorizing preparation of a patent application.
- C. Copy of email sent from Harrity & Snyder, LLP to inventor along with the draft application.
- D. Copy of letter from Harrity & Snyder, LLP to AMD dated October 17, 2002 enclosing application, Declaration/Power of Attorney and Assignment documents.
- E. Copy of letter from AMD to Harrity & Snyder, LLP dated November 7, 2002 enclosing executed Declaration/Power of Attorney and Assignment documents.

EXHIBIT A

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Friday, August 16, 2002 TDG Patent Harvesting Session: Double Gate AMD INVENTION DISCLOS	MAR 0 8 2	# 4105	Rec'd date
This invention applies to: Project IMPORTANT Please identify any potent List 2 to 5 key search words related to 1	ct:, Product:	☐, Process: ☐, Tech	nnology [], Other [],
Working title of invention: Doub	e-(rate Fi	infet with	Separate hates
created by Chemic	ial- Mech	anical Polish	ung (CMP)
→ INVENTOR/SESSION PARTICIPA	NT ADDRESS I	INFORMATION IS ON	NEXT PAGE (1A)←
Inventor's signature : Shibly	Sadigne	Almed	date:
Inventor's printed full name: 51416	LY S. At	1MED Citi	izenship:
Employee #: Extension:	Mail stop:	Home telephone:)
AMD email address:		AMD office	FAX:()
Division: Directorate:]	Dept #: De	pt: Manager:	
Residence address:			
Post Office address:			
	``		
Co-Inventor's signature:	ra Wana		date:
Co-Inventor's printed full name:			Citizenship:
Employee #: Extension:		Home telephone:)
AMD email address:		AMD office	FAX:()
AMD email address:	Dept #: De	ent: Manager:	
Residence address:			
Post Office address:		()	
O			
Co-Inventor's signature :	in Ju		date :
Co-Inventor's printed full name:	1 (litizenship:
Co-Inventor's printed full name: Employee #: Extension:	Mail stop:	Home telephone:()
AMD email address:			
Division: Directorate: I	Dept #: De	nt: Manager:	- ;
Residence address:			
Post Office address:			
Co-Inventor's signature :			date :
Co-Inventor's printed full name:		C	Citizenship:
Employee #: Extension:	Mail stop:	Home telephone:)
AMD email address:			
Division: Directorate: I	Dept #: De	pt: Manager:	· · · · · · · · · · · · · · · · · · ·
Residence address:			
Post Office address:		****	

State total number of inventors here:____. If there are more than four inventors, insert duplicate page 1.

Friday, August 16, 2002 TDG Patent Harvesting Session: Double Gate								
AMD I	NVENTI	ON DISC	LOSURE	TLD	ID#		Rec'd date	
Identify kr	nown relevar	nt art (patents,	publications	, other info	rmation):			
State the p	roblem solv	ed by the inve	ention: Co	reate which	two s	se par	ete gate	s for flexibilit
Brief descr pages, rep	orts and dra		e helpful in d	escribing/	understandin	g the inven	e AMD patent tion):	t notebook
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Friday, August 16, 2002 TDG Patent Harvesting Session: Double C	Gate MAR 0 8 2015					
AMD INVENTION DISCL	OSURE	Rec'd date				
Advantages (check all that apply):						
simplifies manufacturing	improves accuracy / precision	reduces component parts				
<u> </u>	es cost of manufacturing improves reliability improves signal to noise rational improves signal impr					
improves density	improves efficiency provides new functional					
increases operating speed	increases operating range	other, explain below				
(emphasize technical advance in the c	us moustred against thrown arty.					
inventors by the local AMD site Tech Please attach copy of first written des description was discussed. Please attach copy of first drawing(s) Describe any external disclosure of in	scription(s) of invention, with dates, of invention, with date(s).					
Does plan exist to publish, disclose o	or sell? No ., Yes ., If yes, w	here and when?				
Was invention jointly developed with If yes, Company name	-					
If yes, Company name If yes, name of AMD business contact	et and development contract no					
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Background

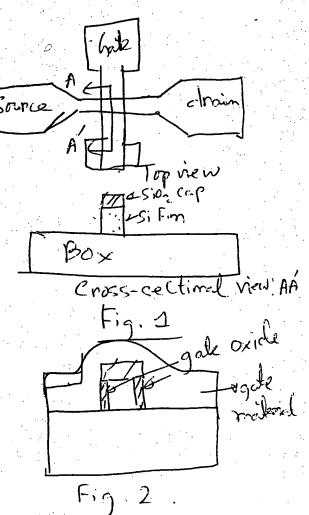
Back ground to Double- hold MosfeT is considered the most scalable of all cmos structures In the past. process complexity posed a significant barrier to the fabrication of Dh devices. The infroduction of the fabrication of Dh devices. The infroduction of FinfeT simplified the process flow and make it compatible with conventional CMOS process. However compatible with conventional CMOS process. However in all the reported result works on FinfeT, two grads in all the reported result works on FinfeT, two grads are ted up connected together. In this disclosure a new fabrication is proposed to achieve separate a new fabrication is proposed to achieve separate a new fabrication is proposed to achieve separate gales, the different gales in FinfeT. In case of separate gales, the different bias can be applied to the gales, which will give bias can be applied to the eircuit design.

Description of process flow-

1) First the active layer is defined of

2) Then the gale exide is graves, and gate material is deposited. (Fig. 2)

3) the gotes are defined by lithernaphy and the actively redesides are selectively redeminds are selectively etched.



9) Gate material is left on top of cap oxide layer Then Conschenical This excess gate moderal is poliched from above the CAP aich. Separate centacts can be post cracked for the gate [Fig. 3] -5) The gotes can be biased ba different separately to give provide more Hoxibility to circuit design. - I hote 1 topriew Thote?

EXHIBIT B





P.O. Box 3453 Sunnyvale, CA 94088-3453 Tel (408) 732-2400

August 29, 2002

Via Federal Express

Glenn Snyder, Esq. Harrity & Snyder, L.L.P. 11240 Waples Mill Road Suite 300 Fairfax, VA 22030

AUG 3 0 2002

Re: TDG Double Gate Patent Harvesting Session - August 16, 2002

Dear Glenn:

Attached are a spreadsheet and hard copies of invention disclosure forms (IDFs—2sets) from the TDG Double Gate patent harvesting session held August 16, 2002.

If you have any questions, please feel free to contact me at (408) 749-2114 or via email at winona.orange@amd.com.

Best regards,

Winona C. Orange

Paralegal

Technology Law Department

Phone: (408) 749-2114 (or 800/538-8450, x42114)

Fax:

(408) 774-7483

Email:

winona.orange@amd.com

Enclosures

EXHIBIT C

Alan Pedersen-Giles

From:

Alan Pedersen-Giles [apgiles@harritysnyder.com]

Sent:

Tuesday, October 01, 2002 10:41 AM

To:

shibly.ahmed@amd.com

Subject:

Draft patent application -- AMD refs. H1105, , H1159, and H1169 -- Our ref. 0020-0068







application.p...



New appl.

0020-0068.doc Dear Shibly,

Enclosed are a draft patent application, drawings, and an accompanying cover letter, the first in Word and the latter two in PDF format. Please review, and ask your fellow inventors to review, this application for accuracy and completeness. Please send me your comments, preferably before October 8, 2002.

If you have any questions or concerns, please do not hesitate to call or e-mail.

Best Regards, Alan Pedersen-Giles

Harrity & Snyder, L.L.P. 11240 Waples Mill Road, Suite 300 Fairfax, Virginia 22030 571-432-0809 (Direct) 571-432-0808 (Facsimile) apgiles@harritysnyder.com

EXHIBIT D

HARRITY & SNYDER, L.L.P.

MAR 0 8 2005

AN INTELLECTUAL PROPERTY FIRM

October 17, 2002

Ms. Winona Orange
Advanced Micro Devices, Inc.
One AMD Place
M/S 68

Re:

P.O. Box 3453 Sunnyvale, CA 94088-3453 VIA FEDERAL EXPRESS

11240 WAPLES MILL ROAD

TELEPHONE: (571) 432-0800 FACSIMILE: (571) 432-0808

FAIRFAX, VA 22030

SUITE 300

Final Draft Patent Application

Title: DOUBLE GATE SEMICONDUCTOR DEVICE HAVING

SEPARATE GATES

Inventors: Shibly S. AHMED et al.

AMD Ref. No.: H1105 Our Ref. No.: 0020-0068

Dear Winona:

Enclosed are Declaration/Power of Attorney and Assignment documents for the patent application referenced above, along with the application. Please have the inventors execute these documents and return them to us for filing in the U.S. Patent and Trademark Office. Also enclosed are Taiwanese Oath and Assignment forms.

We are not aware of any bar dates relating to this application.

We will send you a paper copy of the application and the other executed documents, along with a disk copy of the application in both U.S. and PCT formats, after we file the application in the U.S. Patent and Trademark Office.

Thank you for allowing us to assist you in this matter.

Sincerely,

Alan Pedersen-Giles

la Palery- Slo

APG:ac Enclosures

EXHIBIT E

Via Federal Express



AMD

One AMD Place P.O. Box 3453 Sunnyvale, CA 94088-3453 Tel (408) 732-2400

November 7, 2002

Alan Pedersen-Giles, Esq. Harrity & Snyder, L.L.P. 11240 Waples Mill Road Suite 300 Fairfax, VA 22030

RE:

Our Reference:

H1105

PRIORITY CODE:

Α

Your Reference:

0020-0068

Title:

"DOUBLE GATE SEMICONDUCTOR DEVICE HAVING

SEPARATE GATES"

Inventor(s):

Shibly S. Ahmed, Haihong Wang and Bin Yu

Dear Mr. Pedersen-Giles:

Enclosed please find the executed formal paperwork for the above-referenced case, together with the drafted application and drawings.

The executed Taiwanese Oath and Assignment form will be kept in the respective file here at AMD.

Please contact Dick Roddy for instructions on when to file this case.

If you need further assistance, please contact Winona Orange, the paralegal handling this AMD case.

Sincerely,

Terri Bicknell

Senior Administrative Assistant

Technology Law Department

/tb

Enclosure(s)